Conducting undergraduate research activities in a remote environment

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Abstract: In this work, which is intended to be a Work in Progress Paper in the Innovative Practice Category, the remote environment that was used to supervise students and conduct research tasks as part of an electrical engineering capstone team-based student project is described. While the students successfully completed their projects, more needs to be done to mitigate the negative effects of students feeling isolated while working in a remote environment.

Keywords-Undergraduate research, remote environment, remote testing, FPAA, QIF, Analog to Digital Conversion, gm/ID, OPAMP, stochastic resonance, analog XOR

I. Introduction:

The typical capstone engineering experience for electrical engineering students at the author's institution has been described in previous work [1]. The important parts of the experience related to this work are that the projects are team-based (no fewer than two students per group), with the students either developing their own project or participating in a faculty's research project. The authors' institution is well funded so that the students do not have to purchase equipment, and in many cases, do not have to pay for supplies. Due to the pandemic, and the county-level shelter in place order, and the university's safety plan, students were not allowed to use existing equipment or use any on-campus resources that the students had planned to use to complete their project. This was a significant constraint on the capstone project experience [2].

Downgrading the group's project to simulation only would have prevented the students from meeting critical learning objectives, especially the development of advanced "debugging" skills. Given that the importance of hands-on projects on student learning cannot be overstated, an environment was developed to allow students to work remotely in an authentic manner. (Some remote learning environments constrain the measurement to a prebuilt circuit, which does not allow for debugging [3-5].)

II. Methods:

To create an environment that the students could use to conduct authentic research activities [6,7], a remote system consisting of an ADALM2000 from Analog Devices [8], a field-programmable analog array (FPAA) from ANADIGM [9] were connected to PC that was accessed remotely using the RDP protocol. The ADLAM2000 is a computer-controlled function generator, power supply, voltmeter, oscilloscope, system analyzer (Bode plot), and spectrum analyzer. The FPAA is a field-programmable analog array (from ANADIGM [9] which is a reconfigurable system that uses switched capacitor technology to change the time constants of analog system building blocks. The interconnections of various analog blocks such as integrators, summers, and gain stages can be also be configured like a FPGA (Field Programable Gate Array). (See fig 1.)

Given the short time frame to produce a remote research environment, videos were created and posted to YouTube so that students could learn how to use the remote environment quickly. These videos were critical to passing on information about the new tools from the author to the students because prior to the pandemic, the author did not have any experience using the ADALM200 or the FPAA development kit prior to the shutdown order.

These two boards were accessed remotely via the remote desktop protocol (RDP) to configure analog design blocks to study small neural networks composed of quadratic and fire spiking neurons.

The quadratic integrate and fire (QIF) neuron is the least resource-intensive spiking neuron and thus is an excellent model to use when investigating true spiking neural networks [10]. The attempted QIF-Based projects were an analog a chaotic attractor [11], XOR function [12], a QIF based analog to digital converter [13], and 45nm medium inversion OPAMP design [14,15] for QIF applications. Although each student was assigned their own project, there were expected to help each other.

The students were given protoboards parts and ADALM2000 test kits to investigate the QIF based XOR, Chaotic generator, and analog to digital converter (ADC) designs before the switch to using the FPAA system. FPAA tutorial videos were created rather than traditional tutorials since each student was doing a different QIF-based project, and this too much time would be needed to create a formal document for each project area.

To complete a 500nm practice OPAMP design and a 45nm OPAMP project design, the student used LTSPICE [16] (publicly available AMI06 technology) and the full custom design suite of tools, and the generic process design kit provided by Cadence Design Systems [17]. The student accessed the CAD tools using the remote desktop protocol (RDP) protocol to log in to Linux machines with the Cadence software installed. The OPAMP design fits into the regular QIF research projects because, ultimately, the authors' research group wants to create its own switched capacitor technology. The OPAMP design did not have a hands-on component given that IC fabrication projects are not possible since MOSIS [18] has stopped supporting free fabrication for student class projects.

To enable students who wish to complete an IC design projects, who have not taken an IC design course, extensive tutorials [19,20] were written for LTspice and Cadence tools. Videos were also created to reduce the time the professor had to spend teaching students IC OPAMP design.

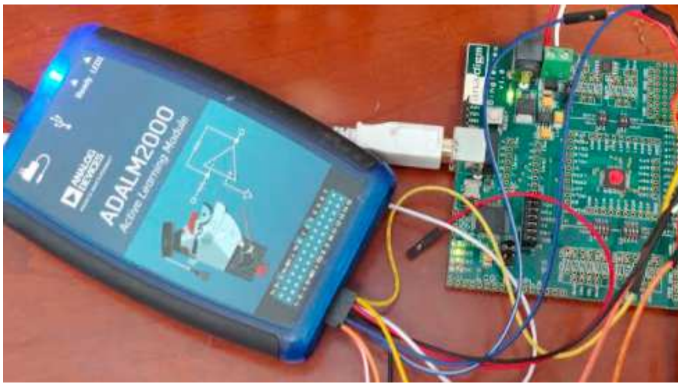

Fig 1: ADALM2000 connected directly to ANADIGM FPAA evaluation board. (PC and power supply not shown.) The FPAA chip was the AN231E04 version.

Traditionally project management consisted of weekly meetings and was mostly to make sure the students were on track. Prior to the pandemic, the advisor was not satisfied with this system because although the students would complete their projects, their results were not presented well enough for publication. To keep students on track in a remote environment and make sure the results were reliable, a google doc system was used to manage student progress, raw data, spice files, and python code to generate figures. In addition, all tutorials and video links and cited works were uploaded to a shared google drive. Student tasks were assigned in google sheets, where progress would be monitored. Reports were written in google docs. To ensure data or spice files were not "lost," a google drive link to a file was linked in the written report. Bi-weekly Zoom meetings were used to keep in touch.

III. Results and Discussion:

The students were able to build on a breadboard and test with an ADLAM2000 provided by the university, a traditional OPAMP-based QIF neuron and XOR neural network. The the chaotic attractor, and the analog to digital converter were simulated in LTspice as regular OPAMP-based designs. The analog XOR was the only design implemented in the field-programmable analog array due to uncertainty on how to program a reset variable in the chaotic attractor and the fact that the analog to digital converter was too ambitious a project. While the 45nm OPAMP was successfully designed, it was not fabricated due to cost constraints.

While students could use the remote environment to complete realistic senior design projects, one could tell that students felt isolated, and this feeling of isolation affected them negatively. This was apparent when students told me that they had not done much over the summer break or needed more help "getting started." The author did not recognize this initially and mostly tried to make break tasks up into small blocks, with regular due dates. Of course, some students liked working on their own.

Before the pandemic shelter in place orders were given. The goal of the project was to create an analog XOR neural net circuit. Givens students could not work together due to equipment limitations, three additional projects were created: Chaos generator circuit, QIF-based ADC, and OPAMP design.

A. QIF-Based Chaotic Generator:

The chaos generator circuit project was supposed to implement the following differential equations:

$\frac{dx}{dt} = x^2 + a - y$ (1) and

$\frac{dy}{dt} = \frac{b-y}{\tau}$ (2) subject to the reset conditions:

$x \rightarrow q, if\ x > h$ (3) and

$y \rightarrow cy + p, if\ x > h$ (4)

Ultimately this project turned out to be too ambitious because a difficult-to-implement reset circuit needed to be developed (equation 4.).

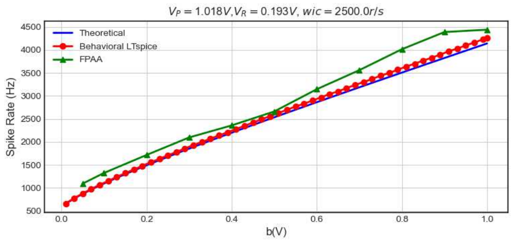

Fig 2: Theoretical, Behavioral, and measured results for QIF neuron. (Multiplier effect.)

This project was changed into a study comparing the theoretical spiking rate to a numerical LTspice model and measured results from an FPAA. The mathematical model of the QIF neuron is given by:

$V = \omega_{ic} \int (aV^2 + b)dt$ (5) subject to a reset condition given by:
$V \rightarrow V_{reset}\ if\ V > V_{peak}$ (6)

Where V and b are functions of time. The variable b is the input to the system. The variable, a, is a scale factor that is also used to make the units match so that V^2 can be added to b. The value of ω_{ic} is the inverse of the time constant of the integrator.

The results of this study can be seen in fig 2. This was a critical study since the chaos generator circuit depends on the accuracy of the ω_{ic}, V_{reset}, and V_{peak}. Preliminary data from the behavioral model showed that the circuit would not spike if the parameters were not set correctly. The fact that FPAA results are higher than predicted will become another research project. Given that the manufacturer of the FPAA, can help create new functionally, and the next student can work with them on the reset issue. There are other chaotic generators, and neural models [21-27] that do not use the QIF or a reset can be studied as well.

B. QIF-Based Analog XOR neural net circuit:

An analog XOR function can be created in a spiking neural net composed of QIF neurons with the algorithm shown in eq. 7. A map of how strong the XOR function is can be seen in figure 3.

$V_{out} = \frac{2}{\pi}\tan^{-1}\prod_{n=1}^{2} W_n X_n + B_n$(7)

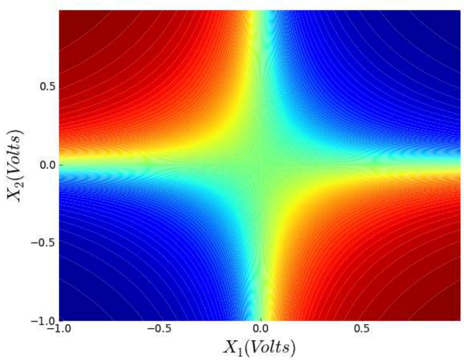

Fig 3: Output of QIF floating point neural net showing XOR identification function. (Values digitized in 100 colors.) W_1= -3.26V, B_1= 0, W_2= 3.34, B_2= 0V

Figure 3 shows the complete FPAA circuit that implements the analog XOR function. Each QIF neuron is completed of a resettable summing integrator, summing low pass filter, and a multiplier. To implement the complete XOR function, two FPAA chips are needed, which were not available. Figure 4 was created with one FPAA, and each signal represents is the output of one neuron. The XOR function was varied by post-processing these two signals in python.

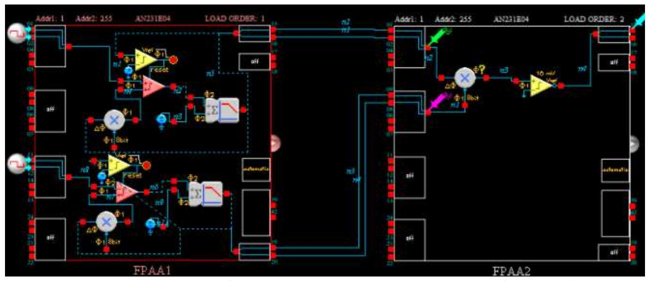

Fig 4: FPAA schematic of QIF based XOR circuit. (Note final multiplier is not shown.) The trained network values are b_n=0, W_1=-1, W_2=1.

Fig 4 shows the typical tangent shape of a QIF with a peak voltage of 951mV, reset voltage of 185mV. When these two signals are passed through a multiplier and then a comparator, the network will give a high value when only one input is spiking. This project was the most successful in terms of measured results because the author had experience with this type of network before the pandemic.

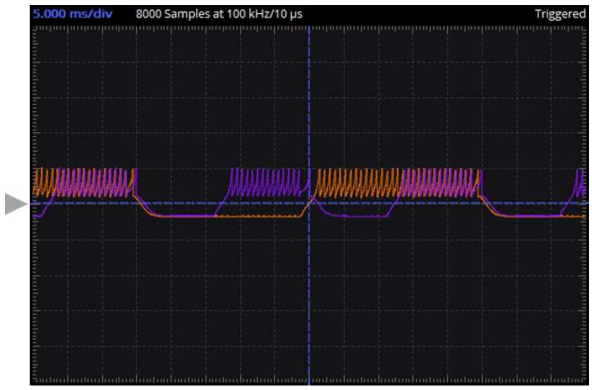

Fig. 5: Transient measurements of core XOR function implemented in FPAA prior to the multiplier of the two output functions. Input b is a square wave at 0.1V. The grey triangle on the left-hand side of the graph is centered at 0V, the horizontal divisions are 10µs/div, vertical divisions are 500mV/div. The integration constant (ω_{ic})is 2500r/s, V_{peak}=951mV, V_{reset}=185mV, and spiking rate is 1.3kHz.

C. QIF-Based Analog to Digital converter with Stochastic resonance:

A one-bit ADC based on the QIF neuron was simulated in LTspice. The one-bit ADC worked by applying the signal to be digitized for a finite period and detecting if a spike occurred. If a spike occurred, then the output was set to high. The ADC was characterized without noise and with white noise added to the input. The noise was added to improve the performance of the ADC by using the stochastic resonance effect. The quantization errors can be seen in Fig. 6. The quantization error with 20% added noise seems to have a lower quantization error.

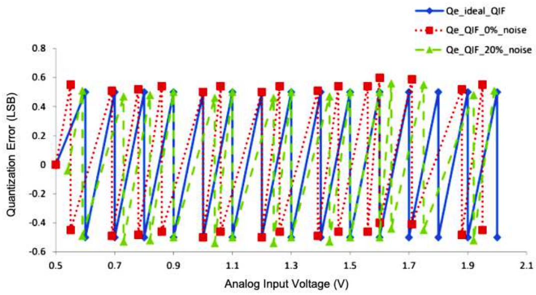

Fig 7: Quantization error of the QIF ADC.

The next step for this project would be implementing the ADC with the FPAA and comparing its performance to the built-in SAR ADC.

D. 45nm OPAMP design for QIF application:

A student designed two OPAMPS in moderate inversion. One was a 500nm design, which was done to familiarize the student with setting a bias current modeling the open-loop gain, gain bandwidth, and setting the phase margin. The other design used a 45nm generic process design kit. The OPAMP topology for both designs can be seen in Fig 6, but only the 45nm parameters are shown. The layout of the OPAMP was not completed since an analog layout tutorial was not created for the student.

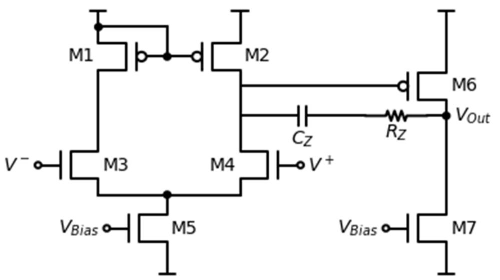

Fig 7: Simplified OPAMP structure L_n=L_p=450nm, W_n(M3, M4, M5, 7)=1.0µm (M1, M2), W_p=3.5µm(M6), W_p=2.2 µm R_z=2k, C_z=7pF, I_{bias}=100uA, V_{power}=±1V. V_{Bias} is provided by a one transistor current mirror (not shown).

The design process consisted of selecting the NMOS transistor width of the differential pair and then using the gm/Id method to select a bias current that biases the NMOS transistors (M2, M3, M5, and M7 in fig 7.) in medium inversion. The MOS widths are then selected to minimize the offset voltage of the differential pair's output when sweeping the positive input and holding the negative input at zero V. M6 is then sized so that both stages have a minimum offset voltage. The DC parameter of gm (transconductance) and r_o (output resistance) were then calculated for each transistor. Given that two-stage OPAMPS have a zero in the right-hand plane, which makes the OPAMP system response unstable when used with negative feedback, C_z and R_z are added to give a phase margin of at least 70°. (This would be -110° measured on a Bode plot.) C_z is found by:

$C_z = \frac{gm_{nmos}}{2\pi GBW_{nofeedback}}$ (8) where the $GBW_{nofeedback}$ is measured from a Bode plot with C_z and R_z removed from the system. Gain Bandwidth (GBW) is the frequency at which the gain goes to zero dB. R_z is set by:

$R_z = \frac{1}{gm_{nmos}}$ (9)

The phase margin would be adjusted by adjusting CZ upward to lower the GBW, increasing the phase margin (stability), or adjusting C_Z downward to increase the GBW and decrease the phase margin (stability).

The simulated extracted parameters for the 45nm OPAMP were V_{offset}= 159µV, GBW= 4.98MHz, phase margin =89° and A_{vol}= 54dB. The nest phase of this project would be to convert it to a programmable switch capacitor design and develop more realistic current mirrors and gain stages.

IV. CONCLUSIONS:

The students were able to complete their senior project in a realistic manner and were able to perform research activities in a remote environment. Although they were successful, there was damage done to the students' psyche due to being isolated. If a remote environment is to be used in the future, more time spent on activities to reduce student isolation is needed. It also might have been better to have two projects with teams of two students. In addition, it was challenging to manage four separate projects.

Although the university anticipates a limited return to campus in the fall, the lessons learned will still be applicable because many of our students commute long distances due to the high price of housing, and have to work to support not only themselves but their families due to the fact that 90% of our students are first-generation college students. If the students need to work remotely (in a hybrid fashion), this could increase undergraduate participation in authentic research activities. Another factor that limits student access to test equipment is that students cannot use the labs at night due to security concerns, given our campus is situated in a central metropolitan area. In addition, there could be more pandemic-like events. For instance, the campus has been shut down due to wildfires several times over the past few years.

The google doc project management method seemed to work well in preserving student work post-graduation. This method worked better than managing a research project using the CANVAS LMS with a permanent course shell. Google docs were able to be used for the project reports but to prepare this manuscript. The content had to be converted to word.

Although students were able to enhance their debugging skills using the FPAA/ADALM2000 system, another option would be to put these two kits in the library for students to borrow in a similar manner to the university's laptop lending program.

Some research areas such as semiconductor fabrication, group robotic projects, or the concrete canoe contest cannot be done remotely. This system helps mitigate this by reducing the number of students on campus, thus allowing on campus only those students whose project cannot be completed in a remote environment.

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